SPN NO.:

ET -11511/ET- 404BL/EV-310BL -23N17

ST. XAVIER'S TECHNICAL INSTITUTE, MAHIM, MUMBAI 400016
DIPLOMA IN ELECTRONICS & TELECOMMUNICATION ENGINEERING
SEMESTER EXAMINATION – WINTER 2017
SEMESTER – V

Time allowed : 3 hours | Marks – 80

MICROPROCESSORS AND PERIPHERALS

Instructions : -

1. Answer to the two sections must be written in separate Answer Book/s.
2. Illustrate your answers with neat sketches wherever necessary.
3. Use of Mathematical tables and Pocket calculators (non-programmable) is permissible.
4. Figures to the right indicate full marks.
5. Assume suitable additional data, if necessary.

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SECTION – I

Q. 1. Attempt any **FOUR.** 16

a) Draw the pin diagram of 8085.

b) Compare EPROM and EEPROM.

c) Draw and explain Bus structure of Microprocessor system.

d) Write a note on fusible link technologies and Anti-fuse technologies.

e) Write an assembly language program to subtract two 8 numbers stored in two successive memory locations.

f) Define following instructions / terms :-

1) Machine Cycle 2) DAA

3) Instruction cycle 4) SVI

Q.2 Answer any **TWO.** 12

a) Describe the following pins of µp 85

(i) ALE (ii) $Io/\overline{M}$

(iii) PUSH (iv) HOLD

(v) INTR (v) S_1 & S_0

b) Draw the simplified flock diagram of µp 85.

c) Write an assembly language program to add 5 Nos. stored in successive locations and store the result.

Q.3 Answer any **TWO.** 12

a) Compare I/O mapped I/O and memory mapped I/O.

b) Draw the interfacing diagram of IC 2764 with IC 8085.

c) Draw internal architecture of 8085 and give any four features of microprocessor.

SECTION – II

Q. 4. Attempt any **FOUR.** 16

a) Explain BSR mode of 8255 with one example.

b) Draw control word form of 8155.

c) Give the comparison between 8155 and 8255 PPI.

d) Draw the internal block diagram of 8155 PPI and explain the function of ALE pin of it.

e) Explain the following pins function :

(i) SOC (ii) ALE

(ii) $\overline{CS}$ (iv) EOC

f) Compare µp 8085 and µp 8086.

Q.5 Attempt any **TWO.** 12

a) Draw the keyboard interfacing using 8279 with µp-8085.

b) Draw the architecture of µp 8086 and list various registers of µp86.

c) List the features of PPI 8279.

Q.6 Attempt any **TWO.** 12

a) Write a program to generate square wave of 50% duty cycle with the frequency of 50KHz at port A of 8255, when an interrupt of µp occurred.

b) Draw interfacing diagram of µp 8085 & DAC.

c) Write a program to read a value of P_A of 8255 and display its square and complement of that square value at P_B and P_C respectively.

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AUTONOMOUS EXAMINATION - SUMMER / WINTER - 2017	
Programme: DETE	SEMESTER : FIVE
Course Code: ET-11511	Course Name: MICROPROCESSOR AND PERIPHERALS
Time Allowed: 03 hours	Maximum Marks: 80

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.

2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.

3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.

4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.

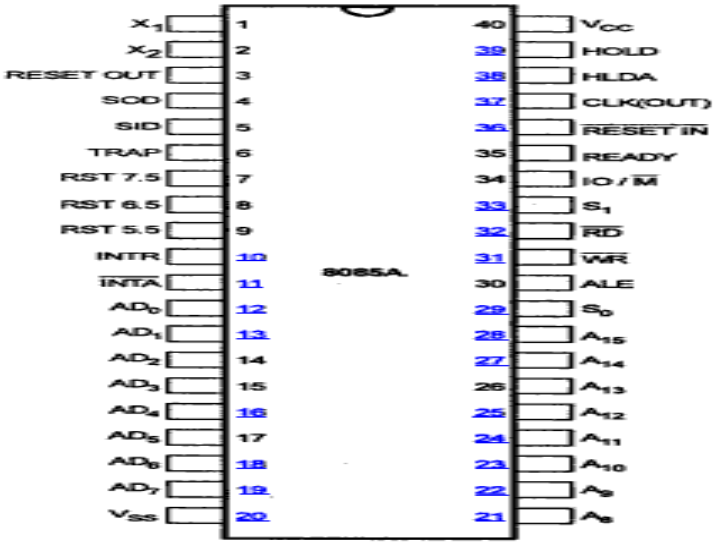
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.

6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.

7) For programming language papers, credit may be given to any other program based on equivalent concept.

Serial No. of Question	Model Answers	Marks

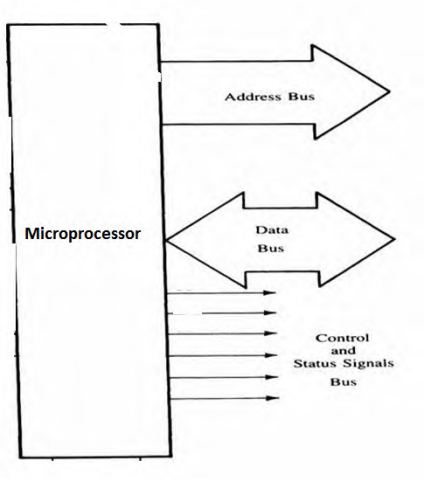
Q-1-a) Pin diagram of 8085



Q1-b)

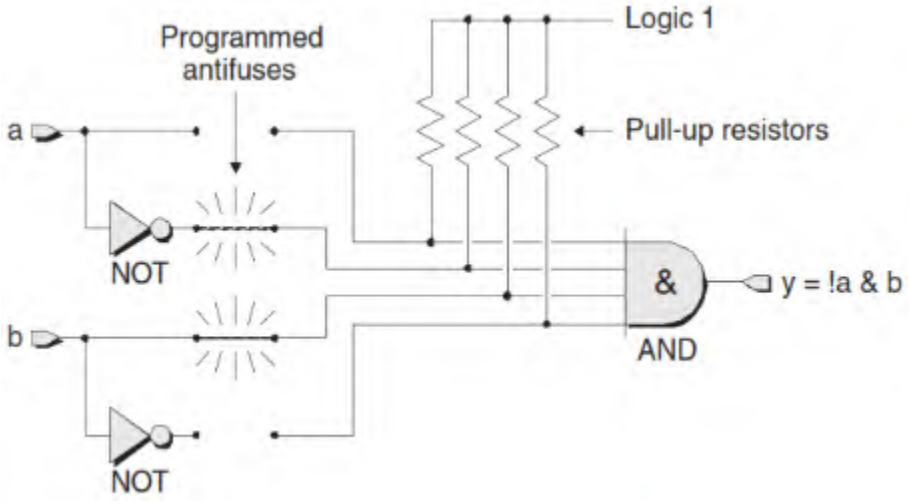
Basis for Comparison	EPROM	EEPROM
Basic	Ultraviolet Light is used to erase the content of EPROM.	EEPROM contents are erased using electronic signal.
Appearance	EPROM has a transparent quartz crystal window at the top.	EEPROM are totally encased in an opaque plastic case.
Erased and Reprogrammed	EPROM chip has to be removed from the computer circuit to erase and reprogram the computer BIOS.	EEPROM chip can be erased and reprogrammed in the computer circuit to erase and reprogram the content of computer BIOS.
Technology	EPROM is an older technology.	EEPROM is a modern version over EPROM.

Q-1-c)



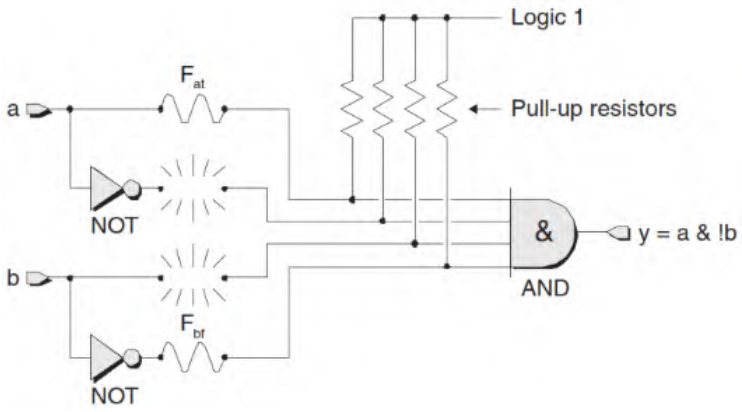
Q-1-d)

Antifuse Technologies

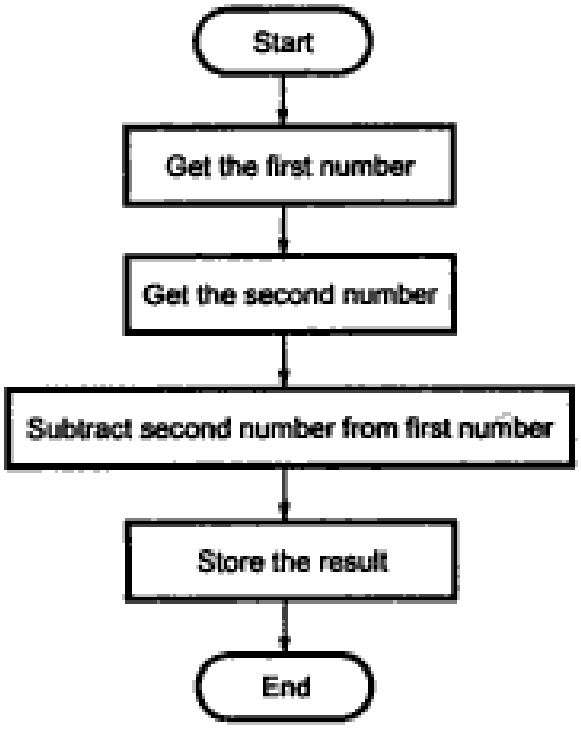
- The unprogrammed device has links which are very high in resistance.
- The compliment of fusible link technology.
- Connections are selectively grown by applying pulses of relatively high voltage and current to the device's inputs.
- Converts highly resistive amorphous silicon to conducting polysilicon.
- 

Fuse Technologies

- All of the fuses are initially intact (after manufacturing).
- Design engineers selectively remove undesired fuses by applying pulses of relatively
- high voltage and current to the device's inputs.
- These devices are one-time programmable, and are not used in FPGAs.



Q1-e)




```
LXI  H, 2000H ; HL points 2000H
MOV  A,M      ; Get first operand
INX  H        ; HL points 2001H
SUB  M        ; Subtract second
                operand
INX  H        ; HL points 2002H
MOV  M,A      ; Store result at 2002H
HLT           ; Terminate program
              ;  execution
```

Q1-f)

Machine cycle ::--

Each memory or I/O operation requires a particular time period, called **machine cycle**. In other words, to move byte of data in or out of the microprocessor, a machine cycle is required.

Instruction Cycle ::--

The fetching, decoding and execution of a single instruction constitutes an **instruction cycle**, which consists of one to five read or write operations between processor and memory or input/output devices.

DAA — This instruction adjusts accumulator to packed BCD (Binary Coded Decimal) after adding two BCD numbers.

Instruction works as follows :

1. If the value of the low-order four bits (D_3 - D_0) in the accumulator is greater than 9 or if auxiliary carry flag is set, the instruction adds 6 (06) to the low-order four bits.
2. If the value of the high-order four bits (D_7 - D_4) in the accumulator is greater than 9 or if carry flag is set, the instruction adds 6(60) to the high-order four bits.

SUI data (8) — This instruction subtracts an 8-bit data given within the instruction from the contents of the accumulator and stores the result in the accumulator.

Operation : A ← A – data (8)

Example : A = 40H,

```
SUI  20H     ; This instruction will subtract 20H from the contents of
               accumulator (40H). It will store the result (20H) in
               the accumulator.
```

Q-2-a)

ALE (Address Latch Enable) : AD_0 to AD_7 lines are multiplexed and the lower half of address (A_0 - A_7) is available only during T_1 of the machine cycle. This lower half of address is also necessary during T_2 and T_3 of machine cycle to access specific location in memory or I/O port. This means that the lower half of an address must be latched in T_1 of the machine cycle, so that it is available throughout the machine cycle. The latching of lower half of an address bus is done by using external latch and ALE signal from 8085.

$IO/\overline{M}$: $IO/\overline{M}$ indicates whether I/O operation or memory operation is being carried out.

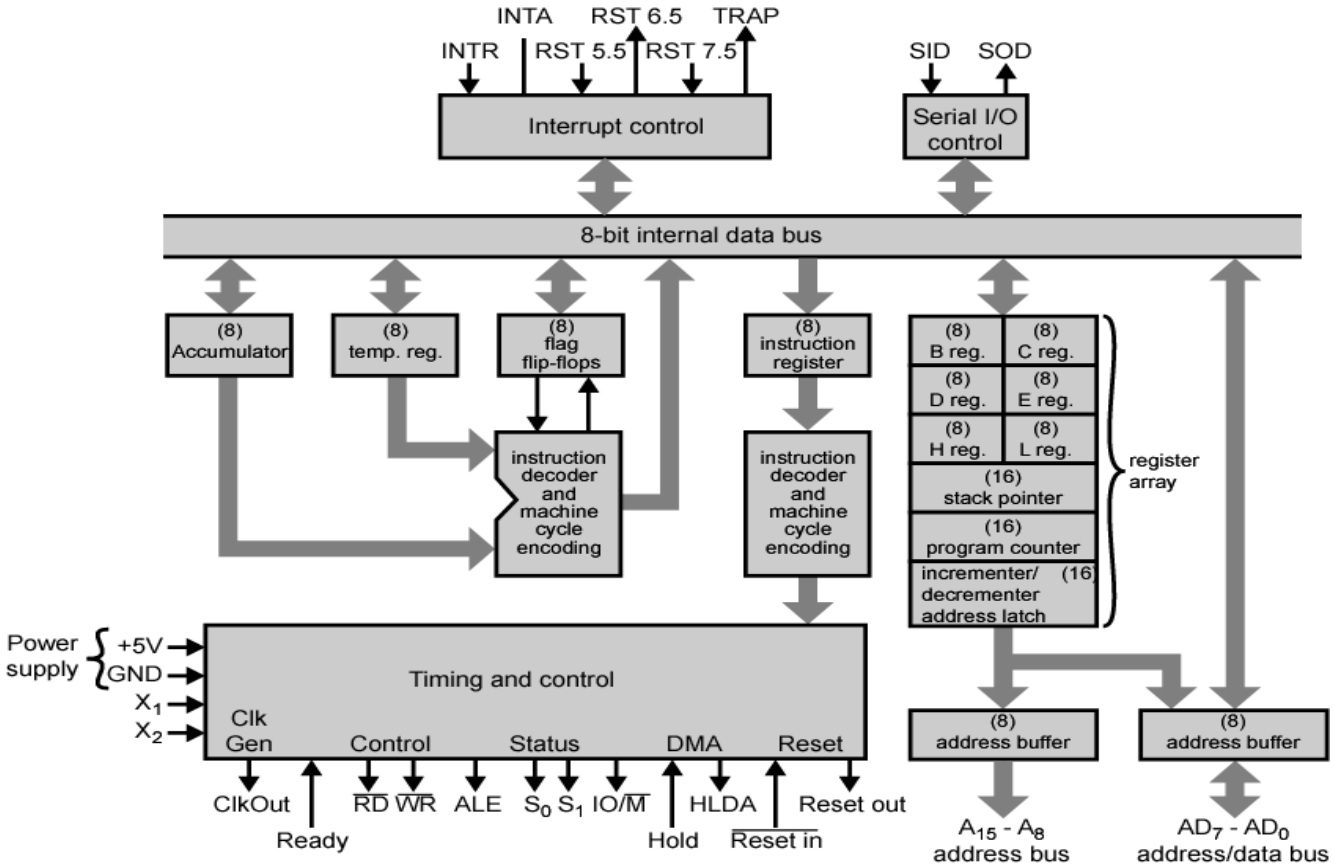
PUSH rp This instruction decrements stack pointer by one and copies the higher byte of the register pair into the memory location pointed by stack pointer. It then decrements the stack pointer again by one and copies the lower byte of the register pair into the memory location pointed by stack pointer. The rp is 16-bit register pair such as BC, DE, HL. Only higher order register is to be specified within the instruction.

HOLD : This signal indicates that another master is requesting for the use of address bus, data bus and control bus.

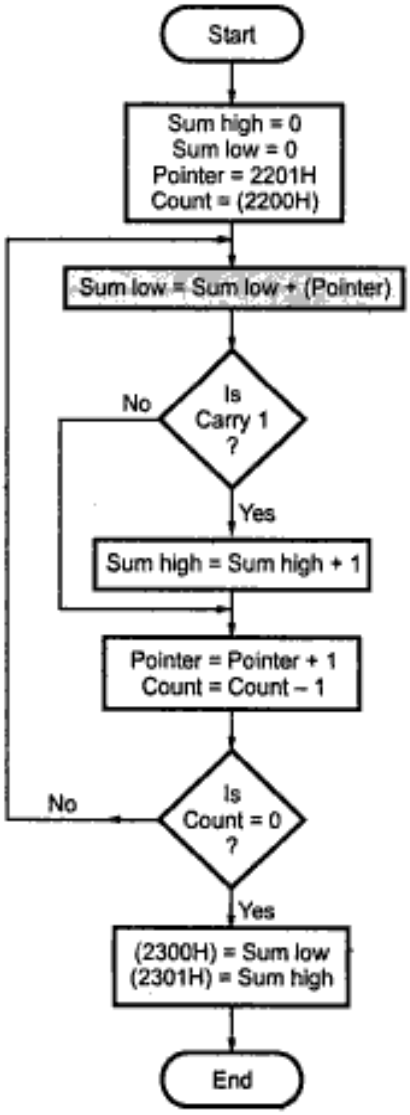
S_0 and S_1 : S_1 and S_0 indicate the type of machine cycle in progress.

INTR : INTR is a maskable interrupt, but not the vector interrupt. It has the lowest priority.

Q-2-b)



Q-2-c) **6 marks for program**




```
        LDA 2200H
        MOV C, A      ; Initialize counter
        LXI H, 2201H  ; Initialize pointer
        SUB A         ; Sumlow = 0
        MOV B, A      ; Sumhigh = 0
BACK :  ADD M         ; Sum = sum + data
        JNC SKIP
        INR B         ; Add carry to MSB of SUM
SKIP :  INX H         ; Increment pointer
        DCR C         ; Decrement counter
        JNZ BACK      ; Check if counter ≠ 0 repeat
        STA 2300H     ; Store lower byte
        MOV A, B
        STA 2301H     ; Store higher byte
        HLT           ; Terminate program execution
```

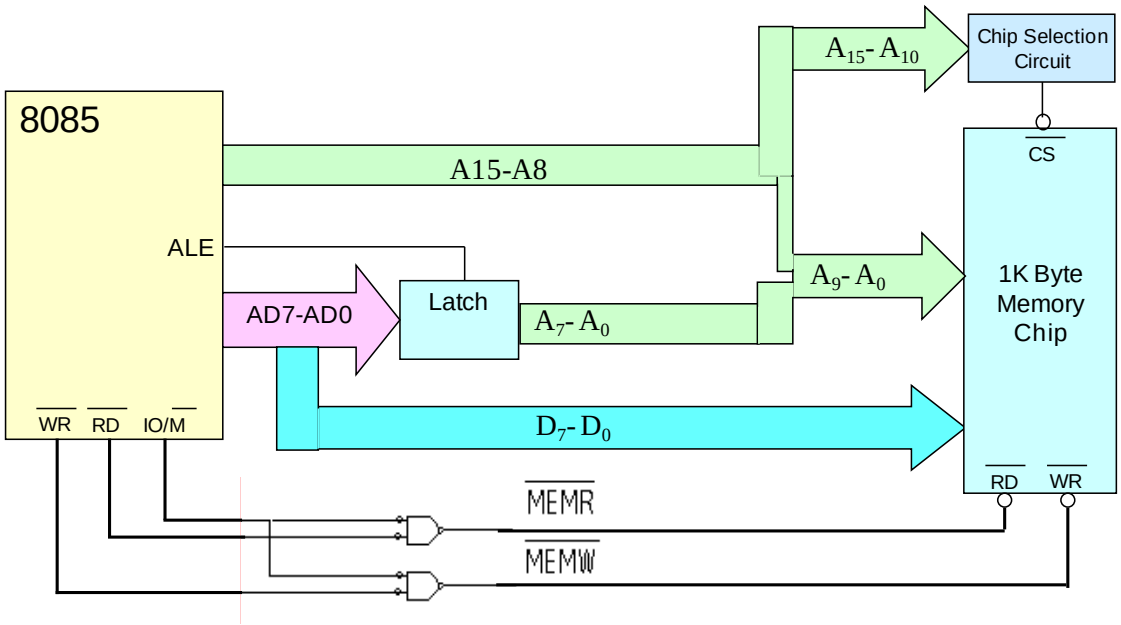
Q-3-a) Memory Mapped I/O :

- In this, there is only one address space. Address space is defined as all possible addresses that microprocessor can generate. Some addresses are assigned to memories and some to I/O devices.
- This technique is suitable for small systems.
- Same address bus to address memory and I/O devices
- Most widely used I/O method
- Access to the I/O devices using regular instructions

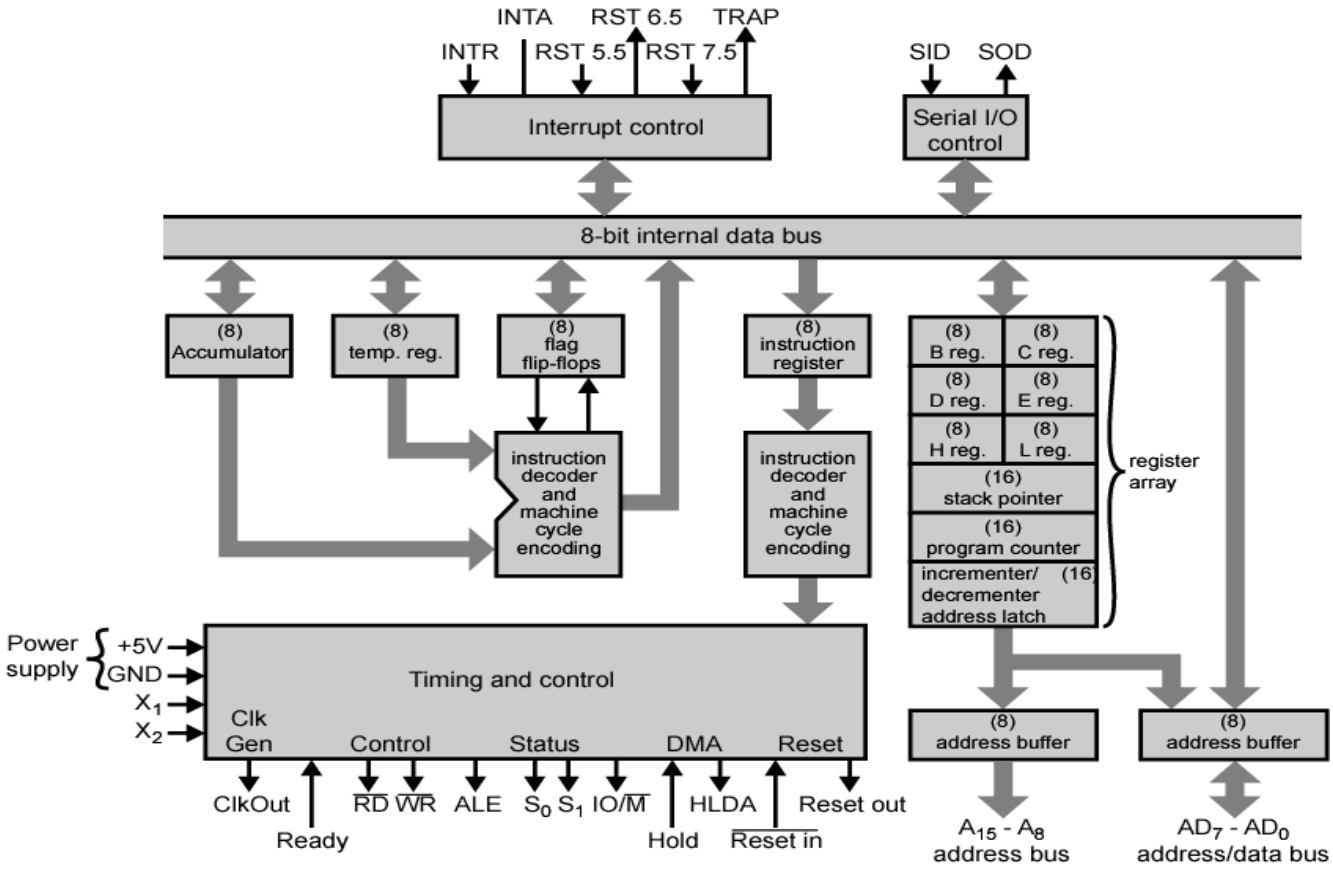
I/O Mapped I/O :

- In this addresses assigned to memory locations can also be assigned to I/O devices. Since the same address may be assigned to a memory location or an I/O device, the microprocessor must issue a signal to distinguish whether the address on the address bus is for a memory location or an I/O device.
- Different address spaces for memory and I/O devices
- Uses a special class of CPU instructions to access I/O devices
- microprocessors - IN and OUT instructions
- This technique is suitable for big size systems.

Q-3-b)



Q-3-c) **2 marks features ; 4 marks for diagram**

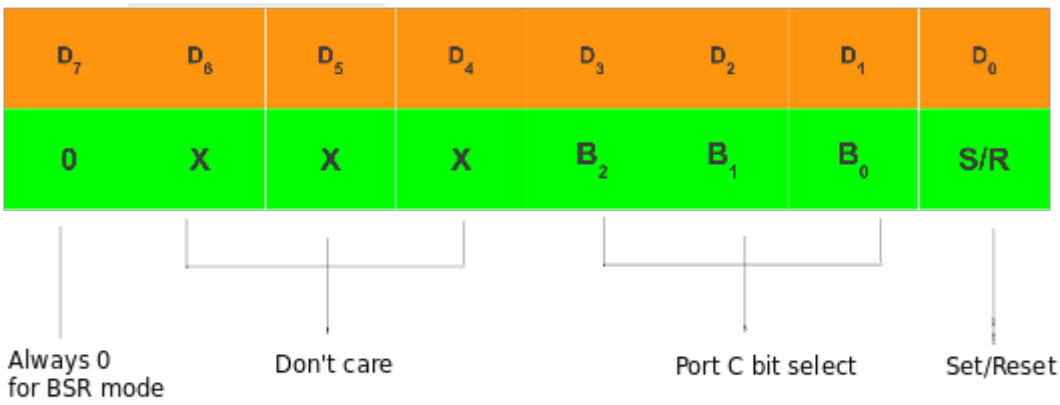


Features :-

1. It is an 8-bit microprocessor i.e. it can accept, process, or provide 8-bit data simultaneously.
2. It operates on a single +5 V power supply connected at V_{CC}; power supply ground is connected to V_{SS}.
3. It operates on clock cycle with 50% duty cycle.
4. It has on chip clock generator. This internal clock generator requires tuned circuit like LC, RC or crystal. The internal clock generator divides oscillator frequency by 2 and generates clock signal, which can be used for synchronizing external devices.
5. It can operate with a 3 MHz clock frequency. The 8085A-2 version can operate at the maximum frequency of 5 MHz.
6. It has 16 address lines, hence it can access (2^{16}) 64 Kbytes of memory.
7. It provides 8 bit I/O addresses to access (2^8) 256 I/O ports.
8. In 8085, the lower 8-bit address bus (A_0 - A_7) and data bus (D_0 - D_7) are multiplexed to reduce number of external pins. But due to this, external hardware (latch) is required to separate address lines and data lines.
9. It supports 74 instructions with the following addressing modes :

   a) Immediate b) Register c) Direct d) Indirect e) Implied

Q4-a)



8255 Control Register format for BSR Mode

Control Word format in BSR mode
The figure shows the control word format in BSR mode.

- This mode is selected by making D7='0'.
- D0 is used for bit set/reset. When D0= '1', the port C bit selected is SET, when D0 = '0', the port C bit is RESET
- D1, D2, D3 are used to select a particular port C bit whose value may be altered using D0 bit as mentioned above The selection of the port C bits are done as follows:

D3	D2	D1	bit/pin of port C selected
0	0	0	PC0
0	0	1	PC1
0	1	0	PC2
0	1	1	PC3
1	0	0	PC4
1	0	1	PC5
1	1	0	PC6
1	1	1	PC7

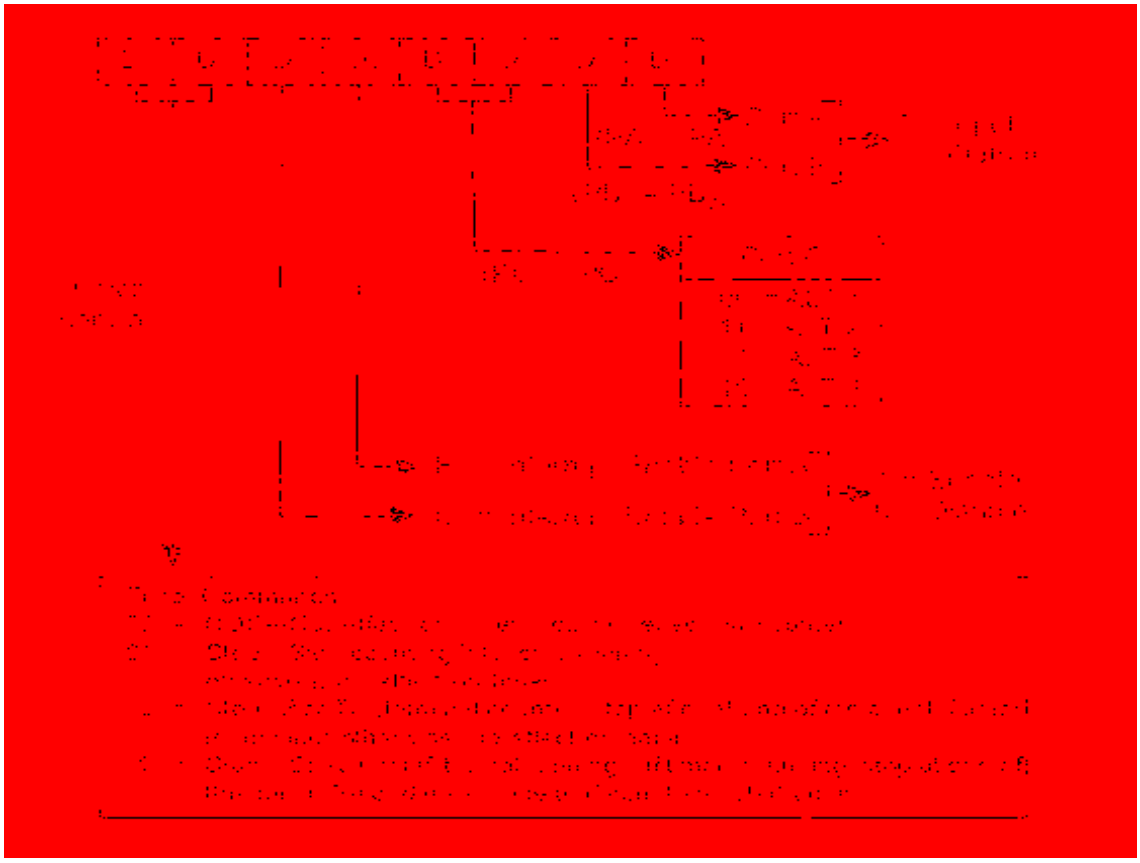
- **D4, D5, D6** are not used.

If the 5th bit (PC5) of port C has to be "SET", then what is the control word?

- 1. Since it is BSR mode, **D7 = '0'**.
- 2. Since D4, D5, D6 are not used, assume them to be **'0'**.
- 3. PC5 has to be selected, hence, **D3 = '1', D2 = '0', D1 = '1'**.
- 4. PC5 has to be set, hence, **D0 = '1'**.

Applying the above values to the format for BSR mode, we get the control word as **"0B (hex)"**.

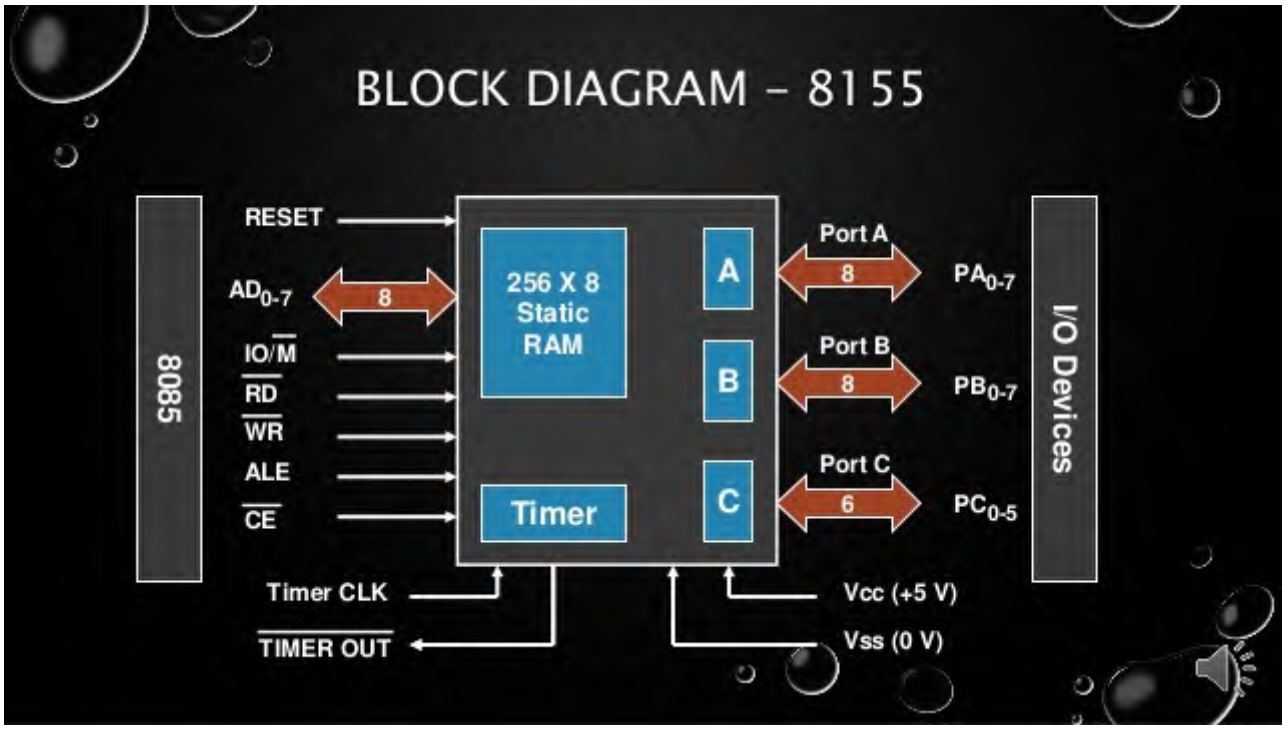
Q4-b)



Q4-c)

- The 8155 is an integrated RAM
- Require A0-A7 address lines
- Inbuilt timer register
- Status register is available
- The 8255 is not having inbuilt RAM
- Require A0-A1 address lines
- Timer register absent
- Don't have status register

Q4-d)



Q4-e)

- SOC ::- this signal pin is use to indicate the start of conversion signal.
- EOC ::- this out going signal pin is use to indicate the end of conversion signal.
- CS ::- active low input signal is to activate the chip.

Q4-f)

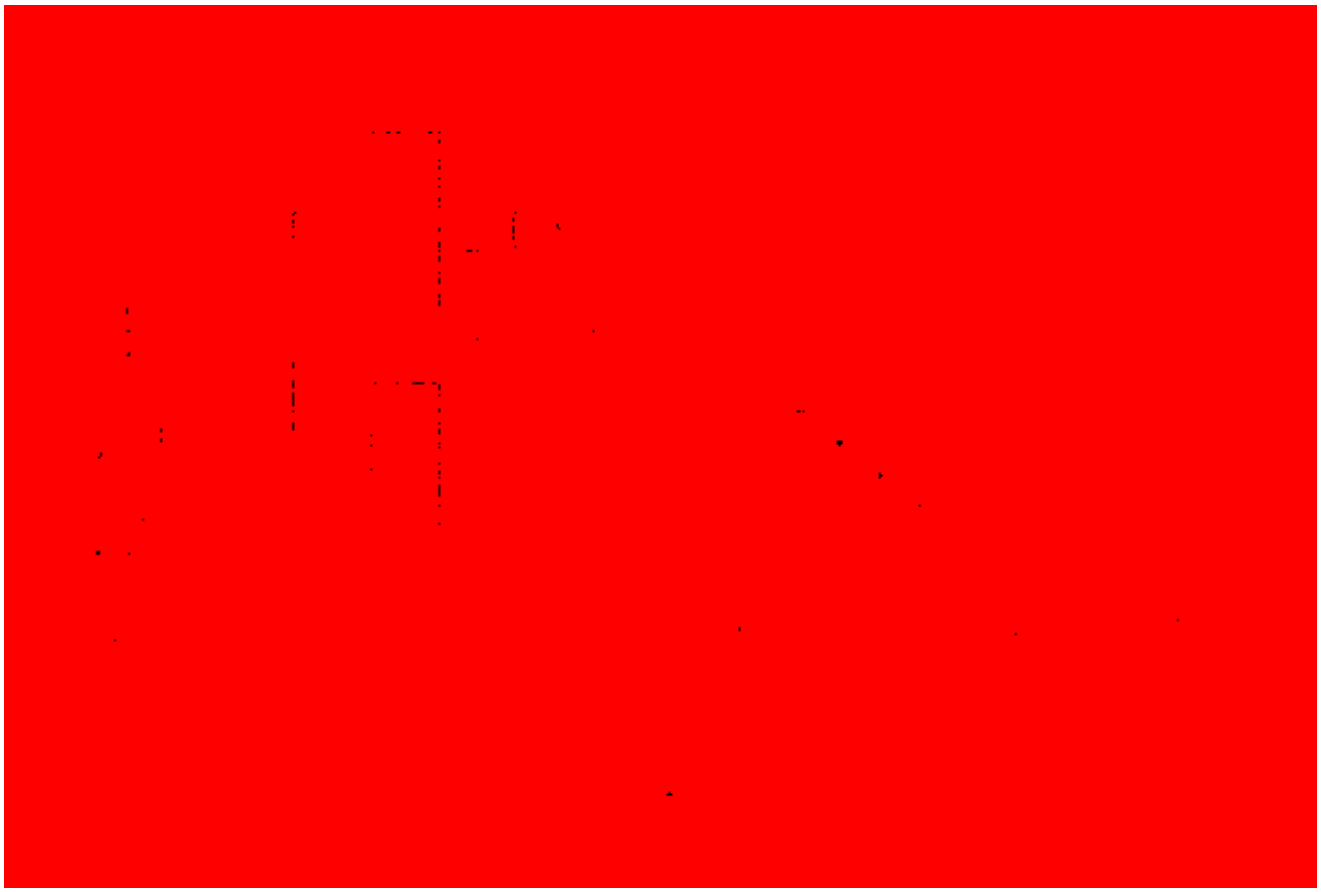
8085 microprocessor	**8086 microprocessor**
• It is 8 bit microprocessor	• It is 16 bit microprocessor
• It has 16 bit address line	• It has 20 bit address line
• It has 8 bit data bus	• It has 16 bit data bus
• clock speed of 8085 microprocessor is 3 MHz	• clock speed of 8086 microprocessor vary between 5,8 and 10 MHz for different versions.
• It has 5 flags.	• It has 9 flags.
• It does not support pipelining.	• It supports pipelining.
• It operates on clock cycle with 50% duty	• It operates on clock cycle with 33% duty cycle.

cycle.

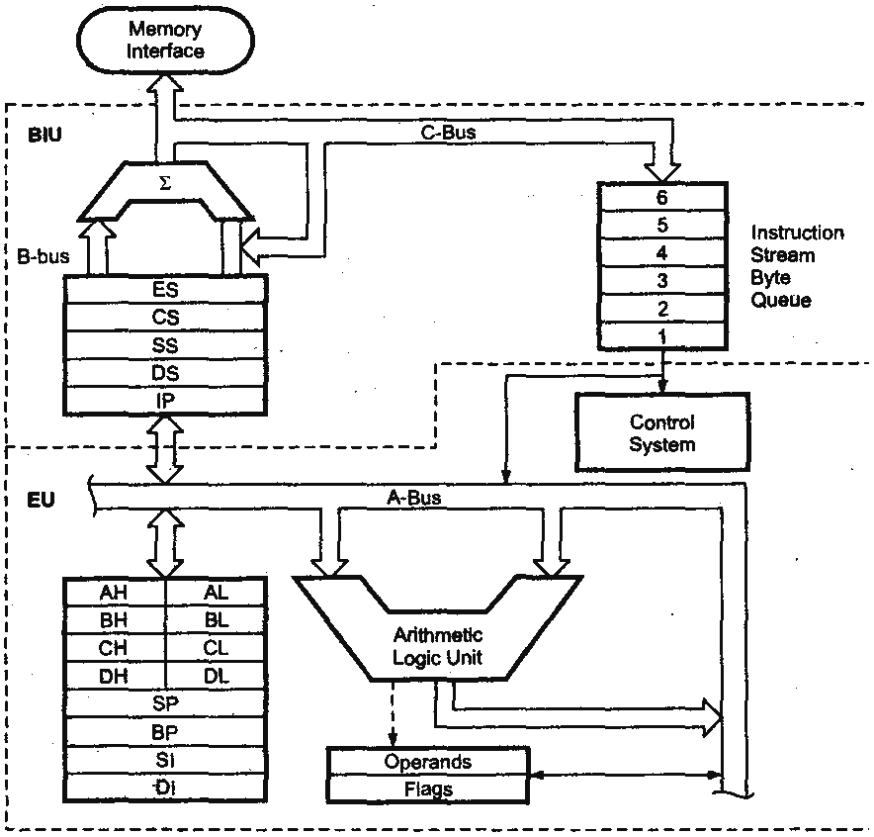
- 8085 microprocessor does not support memory segmentation.
- It has less number of transistors compare to 8086 microprocessor. It is about 6500 in size.
- It is accumulator based processor.
- It has no minimum or maximum mode.
- In 8085, only one processor is used.
- In this microprocessor type, only 64 KB memory is used.

- 8086 microprocessor supports memory segmentation.
- It has more number of transistors compare to 8085 microprocessor. It is about 29000 in size.
- It is general purpose register based processor.
- It has minimum and maximum modes.
- In 8086, more than one processor is used. Additional external processor can also be employed.
- In this microprocessor type, 1 MB memory is used.

Q5 a)



Q5 b)



Q5 c)

8279 has 3 input modes for keyboard interface

i. Scanned keybaord mode
ii. Scanned Sensor Matrix Mode
iii. Strobed Input Mode

8279 has 2 output modes for display interface

i. Left Entry
ii. Right Entry

- It has two key depression modes
  i. 2 key lockout mode
  ii. N key rollover mode
- It has built-in hardware to provide key bounce.
- It provides 8 byte FIFO RAM to store keycodes.
- It provides multiplexed display interface with blanking and inhibit options.
- It provides 16 byte display RAM to store display codes for 16 digits, allowing to interface 16 digits.
- Simultaneous keyboard and display operation facility allows to interleave keyboard and display software.

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Serial No. of Question	Model Answers	Marks
Q6 a)	LXI SP 2000H	
	MVI A, 80H	
	OUT CWR	
G:	MVI A, 09H	
	SIM	
	EI	
H:	JMP H	
	DI	
	JMP G	

Interrupt Subroutine.

```
        MVI A, FFH
        OUT PA
        LXI D, Count for delay
L1:     DCX D
        MOV A, D
        ORA E
        JNZ L1
        MVI A, 00H
        OUT PA
        LXI D, Count for delay
        ~~JNZ L2~~
L2:     DCX D
        MOV A, D
        ORA E
        JNZ L2
        RET
```

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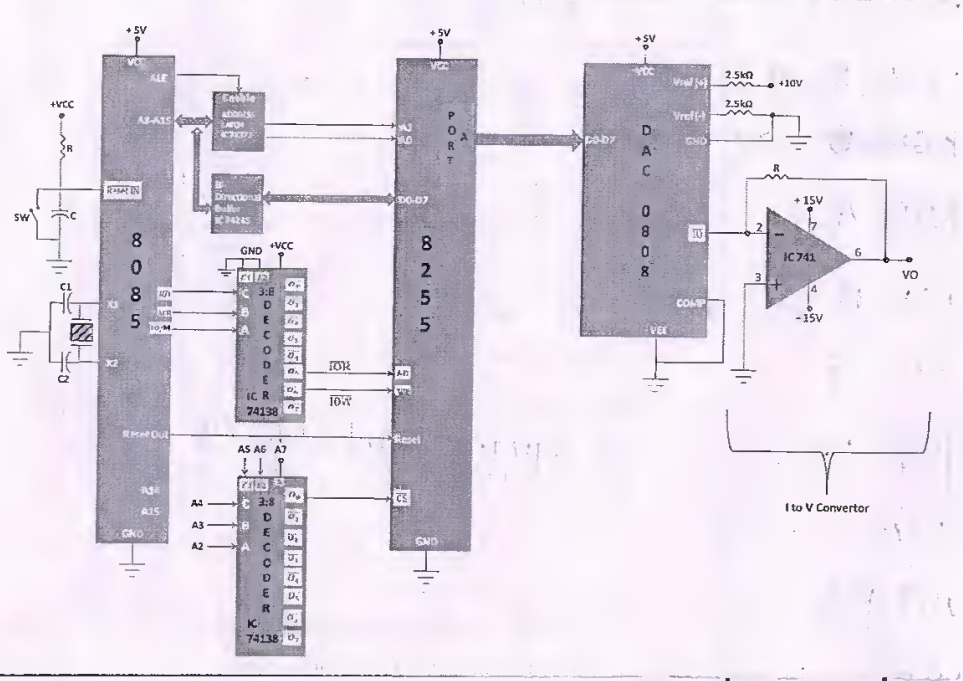
Serial No. of Question	Model Answers	Marks
Q6b)		
Q6 c)	MVI A, 90H	
	OUT CWR	
	IN PA	
	MOV B, A	
	MOV A, 00H	
G:	ADD A	
	DCR B	
	JNZ G	
	OUT PB	
	CMA	
	OUT Pc	
	HLT	